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Single Phase Multi- Level Inverter using Single DC Source and Reduced Switches

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Abstract. In this paper a study of 9-level inverter using single DC source three capacitors of suitable value and 6 IGBT switches as compared to the technologies previously developed, the number of gate driving circuits has been reduced, which leads to the reduction of the size and power consumption in the driving circuits. The proposed type of converter is suitable for high voltage and high power applications. The power loss in the circuit is reduced due to less number of switches which helps to get a better harmonics spectrum. The Simulation of a 9-level inverter with the proposed topology by Sinusoidal Pulse Width Modulation technique has been carried out to minimize the Total Harmonic Distortion (THD) using Mat lab software.

Keywords: Multilevel Inverter, Unidirectional Switch, Cascade Inverter

1. Introduction

Multilevel inverters helps in producing stepped output waveform which results in higher output waveform quality and lower distortion. The first ever introduced topology is the series H-bridge design [1]. This H-bridge topology was followed by the diode-clamped inverter [2–4] which utilizes a bank of series capacitors to split the dc bus voltage. Hybrid multilevel converters have been presented in [5],[6]. In the hybrid topologies, the magnitude of dc voltage sources are unequal or changed dynamically depending upon the need [7]. These converters are very efficient in the size and cost and improve the reliability since less number of semiconductors and capacitors are used in this topology [8]. The hybrid multilevel converters consist of different multilevel topologies which are having unequal value sources of dc voltage magnitude and different modulation techniques [5]. With proper selection of switching devices and technique, the converter cost is reduced.

Before coming to the proposed topology, first lets us discuss some techniques that have been implemented to reduce the number of power switches. As Fig. 1 shows some proposed bidirectional switches. Fig. 1 (a)

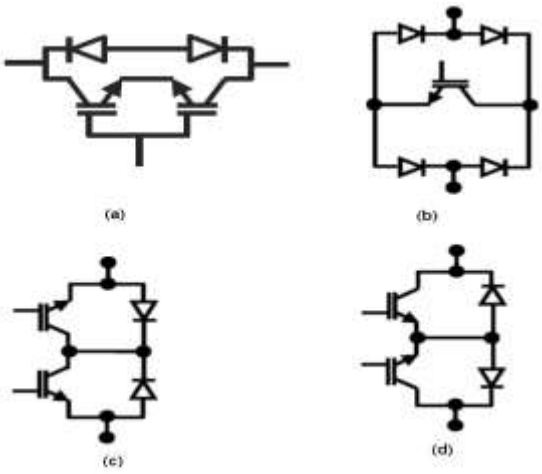

Fig.1: Conventional Bidirectional Switches

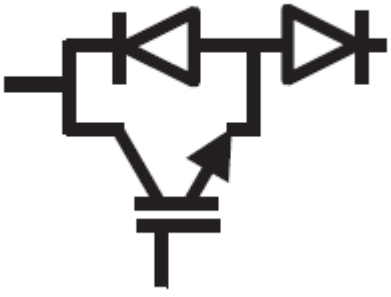

Fig. 2: Unidirectional Switch

Bidirectional switch is used to stop the counter desired direction of current flow [9]. But in this proposed topology Fig 2, unidirectional switch is used. Now comparing both the switches, Fig. 1 (a) is a bidirectional switch, whereas Fig. 2 is a unidirectional switch. Depending upon the requirement we have developed

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Unidirectional Switch (Fig 2) which consists of only 1 IGBT and 1power diode where as in Fig. 1 (a) two IGBT's are used. It aids in reducing the number of switches.

Proposed unidirectional switch as shown in Fig. 2, which is nothing but an IGBT and a power diode in series. The direction of the current will be in the direction of the power diode. For the unidirectional switch shown in Fig. 2, the direction of current will be either to the right or zero.

2. Single DC source Implementation using Capacitors

2.1. Proposed Cell

In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of IGBT switches when compared to ordinary cascaded multilevel inverter. The proposed topology consists of less number of switches when compared to the other familiar topologies. The initial cost reduces because of the switch reduction. So, it looks attractive and an apt one for industrial applications. Proposed circuit is derived from [9] and modified to single dc source and reduces the number of power switches. Here all the capacitors are charged already and then added to the circuit, while the total voltage is provided by the DC source with a small resistance in series to make charging of the uncharged capacitors.

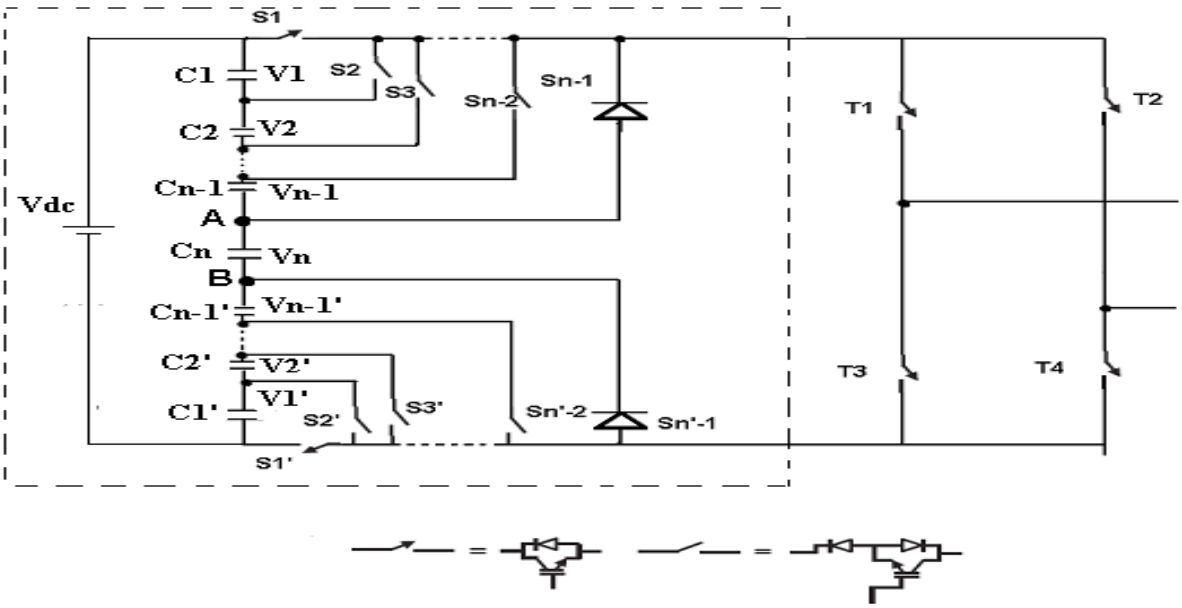

Fig. 3: General Circuit Diagram of proposed Topology

2.2. Topologies derived using above Technique

For same number of voltage levels different kind of topologies could be designed like in fig. 4(b) And fig. 4(c), both are for 7 levels but have slight difference in number of capacitors used and magnitude of DC voltage across the capacitors. Topology shown below uses unidirectional switches in desired places to reduce the number of IGBT used, whereas bidirectional is used in [9]. But cascading is not that simple as our main focus is to reduce the number of power switches and DC Sources. Some proposed cell has been cascaded, like in fig. 5(a), 3 cells has been cascaded, but the thing to notice here is we have not involved the four IGBT H-bridge in each cell, as shown in fig. 5, which is done in conventional cascading technique. Dotted portion shown in fig. 3 is only needed for cascading, we are not using H-bridge is every cell. Only the load consist the four IGBT's H-bridge, which means we are reducing four IGBT's with increase in each extra cell. First thing in cascading the proposed topology is to make sure that each cell is in isolated condition with all switches in off state. For cascading the proposed cell, some rules must be followed. If there is no DC source between point A and B in the first cell, then the corresponding cells could be used, same as the first cell. An illustration has been shown in fig. 5(a).

But if the first cell of the cascade has a DC source between point A and B, then the corresponding cell cannot afford to have a DC source in between point A' and B', A'' and B'' etc. An illustration has been shown in Fig. 5(b). The above set of rules will make sure the proper cell designing and functioning. Because of these rules, we are able to save four IGBTs with increment in each cell. The only disadvantage is if there is any source between point A and B, according to fig. 5(b), then there won't be symmetry between the first cell and the other cells of the cascade, so the calculation won't be straight forward, but it also won't be

complicated. Basically here we are taking all the cells in series and then putting it around Load using H-bridge. For Symmetric cascading, two points should be kept in mind, first is that the first cell should not have any DC source between point A and B, and the second point is, all the DC sources used in the topology should have same magnitude.

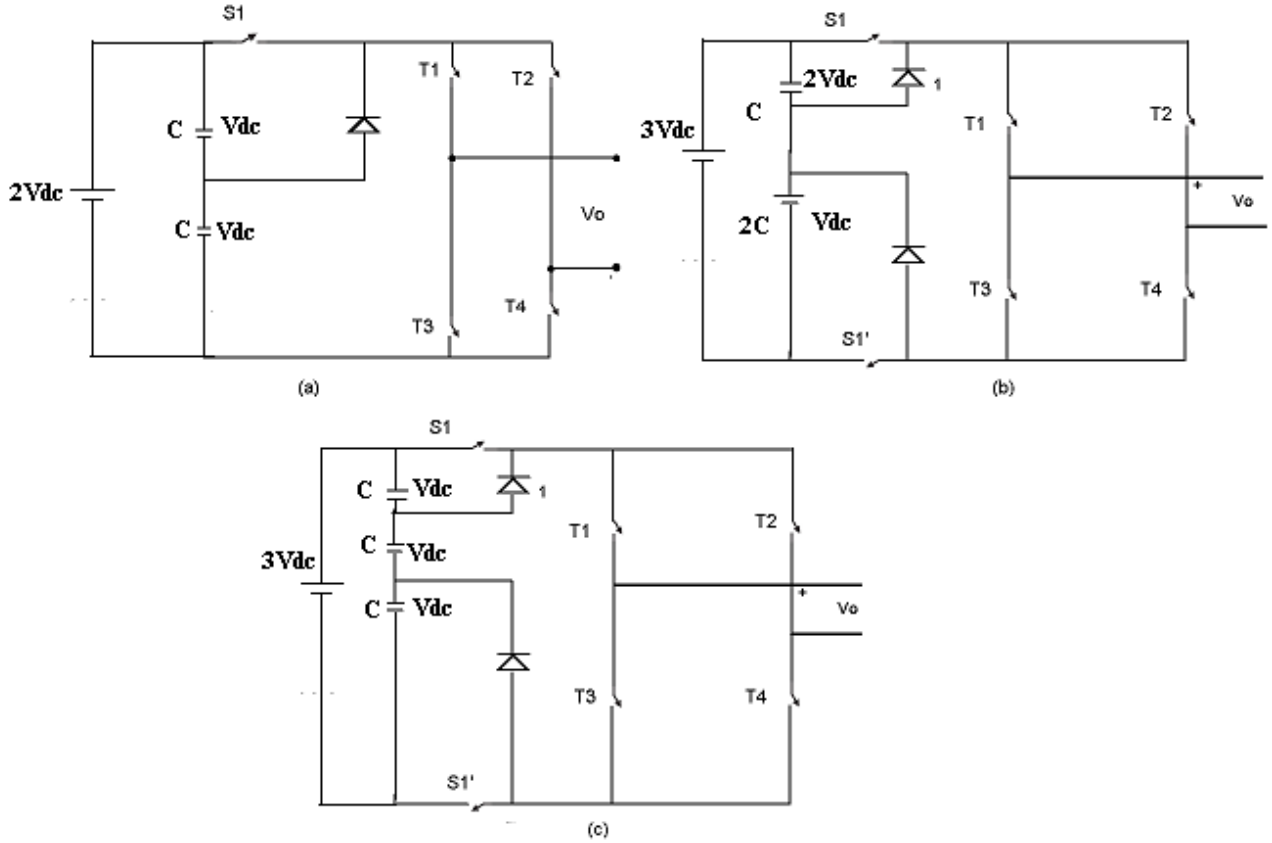

Fig. 4: Single Cell for 5,7 and 7 in (a),(b) and (c) respectively

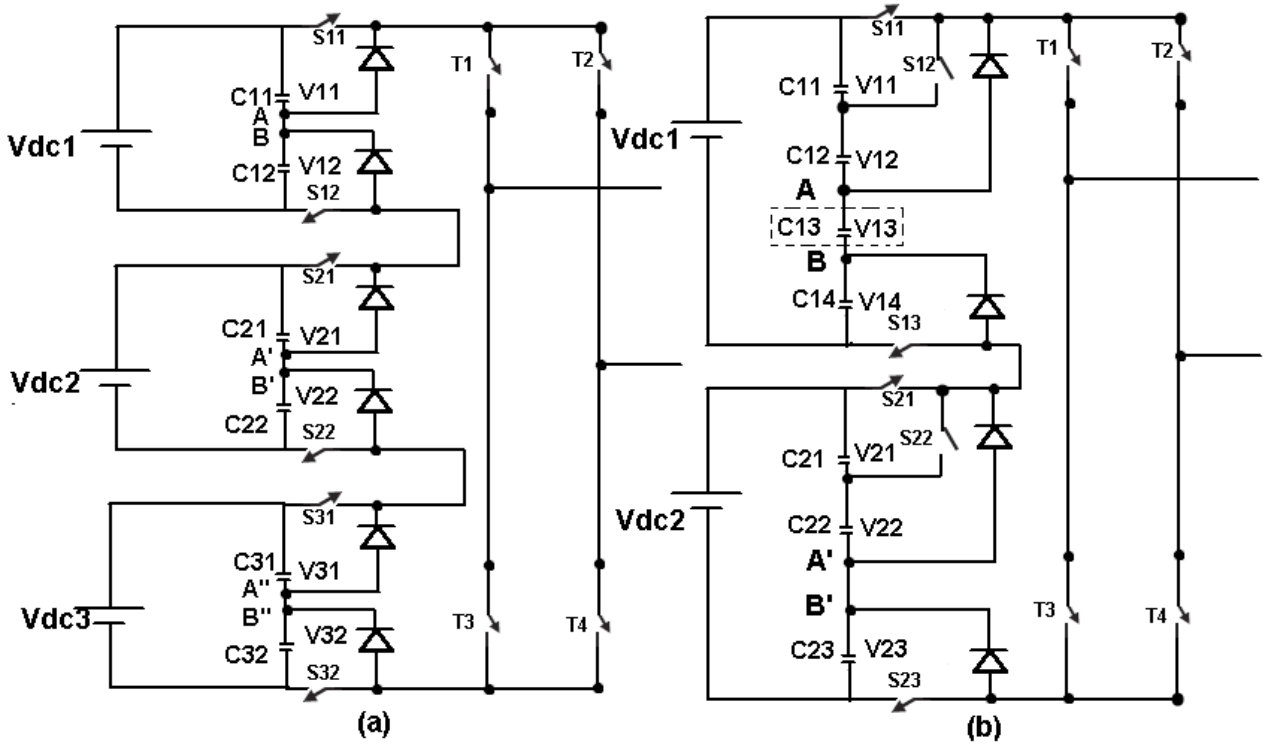

Fig. 5: Topologies from the general Proposed Topology

Asymmetric cascading of cells is done to maximize the number of voltage levels. Let's consider fig 6(a), first cell's voltages V11 and V12 be Vdc and 2 Vdc. Similarly second cell's first voltage source V21 should

have a voltage greater than net voltage of the first cell, that is Vdc +2 Vdc =3 Vdc, it could be 4 Vdc and second voltage source of second cell V22 is 8 Vdc. Similarly goes for the next upcoming cells.

For cell 1

- V11= Vdc
- V12= 2Vdc

For cell 2

- V21= 4Vdc
- V22= 8Vdc

For cell 3

- V31= 16Vdc
- V32= 32Vdc

The above value is to bring maximum level output for fig. 5(a), a maximum of 127 levels we can achieve. So with the help of three DC sources of different magnitude, six capacitors and ten IGBT's, we are achieving 127 levels. For every topology, we can generate a formula like above for any number of level less than or equal to maximum voltage levels. Percentage reduction in number switches for unsymmetrical is even higher. So above results clearly shows the quality and the effectiveness of this topology.

2.3. Topology Proposed for the generation of 9-levels

Simulation results are shown with the help of MATLAB software for proposed topology for 9-level inverter in fig. 7. The results are shown by Pulse Width Modulation control technique. The battery used is of 40 volts chosen for input supply. The load of industries is generally R-L load hence the load connected here is the same R-L load. The IGBT's used in this topology to provide higher stability and reliability to the circuit. In the experimental point of view, the output voltage waveform and the output current waveform are studied and analyzed

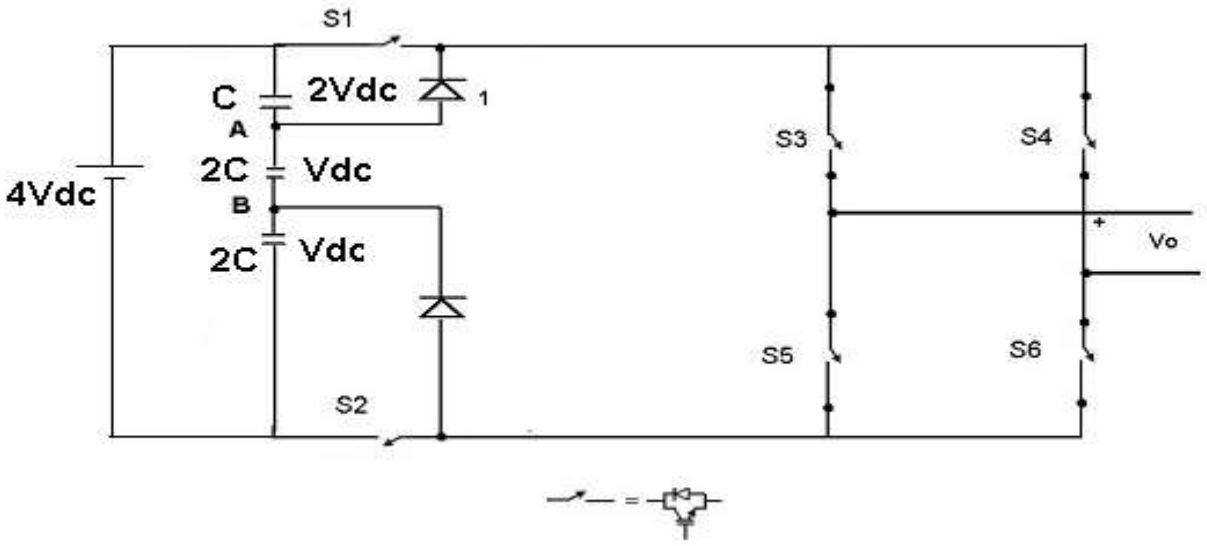

Fig. 6: Proposed Circuit for 9-levels.

Table I shows the firing circuit for the topology shown above (Fig. 6).

TableI

Serial number	Conducting Switches	Output Voltage
1	S2,S6	+Vdc
2	S2,S3,S6	+2Vdc
3	S1,S3,S6	+3Vdc
4	S1,S2,S3,S6	+4Vdc
5	S5,S6	NIL
6	S4,S5	-Vdc
7	S2,S4,S5	-2Vdc
8	S1,S4,S5	-3Vdc
9	S1,S2,S4,S5	-4Vdc

2.4. Results

To evaluate the performance and quality of the proposed multilevel topology in the generation of desired output voltage waveform, a single-phase 9-level multilevel is simulated. The main objective of this proposed topology is to synthesis the output voltage with minimum distortion with respect to the reference voltage. The main drawback to be considered in this proposed topology is that it requires multiple numbers of capacitors whose value should be taken precisely so to maintain a proper balance between charging and discharging. In the experimental point of view, the output voltage waveform and the output current waveform are studied and analyzed. Regarding this, the converter has been adjusted to produce a 50 Hz, 9-level staircase waveform. The results of this are shown in figure7 and figure8.

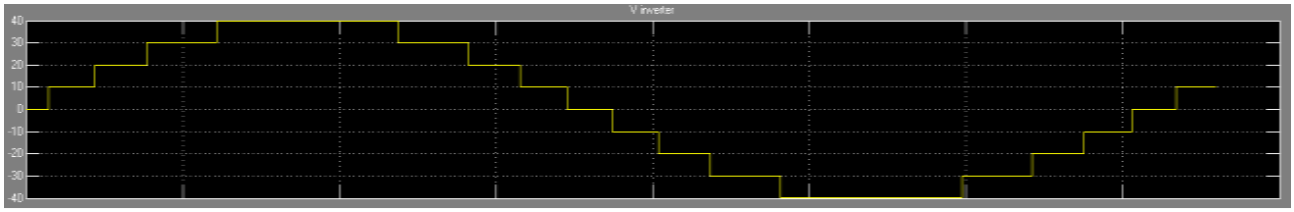

Fig. 7: Output Voltage Waveform

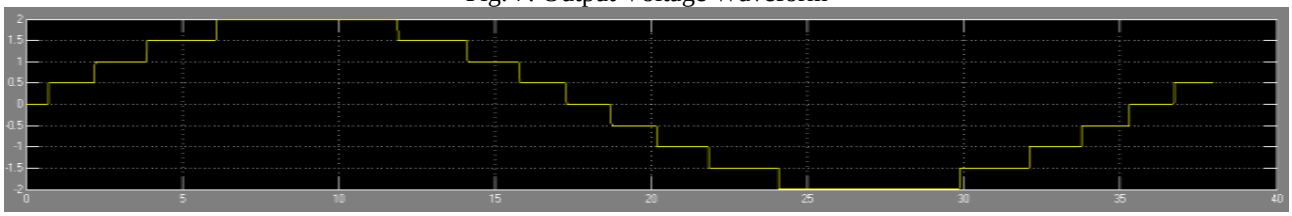

Fig.8: Output Current Waveform

3. Acknowledgements

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4. References

[1] Baker RH. Electric power converter. US Patent 03-867-643; February 1975.

[2] Baker RH. High-voltage converter circuit. US Patent 04-203- 151; May 1980.

[3] Nabae A, Takahashi I, Akagi H. A new neutral-point clamped PWM inverter. In: Proceeding of the industry application society conference; 1980. p. 761–6.

[4] Fracchia M, Ghiara T, Marchesini M, Mazzucchelli M. Optimized modulation techniques for the generalized N-level converter. In: Proceeding of the IEEE power electronics specialist conference, vol. 2; 1992. p. 1205–13.

[5] C. Rech and J. R. Pinheiro, ―Hybrid multilevel converters: Unified analysis and design considerations,‖ IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 1092–1104, Apr. 2007.

[6] C. Rech and J. R. Pinheiro, ―Line current harmonics reduction in multipulse connection of asymmetrically loaded rectifiers,‖ IEEE Trans. Ind. Electron. vol. 52, no. 3, pp. 640–652, Jun. 2005.

[7] S. Lu, S. Marieethoz, and K. A. Corzine, ―Asymmetrical cascade multilevel converters with noninteger or dynamically changing dc voltage ratios: Concepts and modulation techniques,‖ IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2411– 2418, Jul. 2010.

[8] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, ―Multilevel converters: An enabling technology for high-power applications,‖ Proc. IEEE, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[9] Ebrahim Babaei, Mohammad Farhadi Kangarla, Mehram Sabahi, Mohammad Reza Alizadeh Pahlavani,―Cascaded multilevel Inverter using Sub-multilevel cells||Science Direct, in Electric Power System Research 96(2013)101-110.